REMARKS

Claims 1-11 are pending. Claims 1 and 7 have been amended. Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

Entry of this Amendment is respectfully requested since no new issues are raised by entry of the Amendment and it places the application in condition for allowance or at least in better form for appeal.

Claim Objections

The claims 1 and 7 were objected to as containing grammatical errors. Applicant has amended claims 1 and 7 to correct these grammatical errors. Accordingly, Applicant respectfully submits that this objection is moot.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-6 were rejected under 35 U.S.C. § 103(a) over Williams (U.S. Patent No. 6,745,338) in view of Hui et al. (U.S. Patent No. 6,694,463). Applicant respectfully traverses this rejection.

Claim 1 recites, in part, a microcontroller that includes a first switch, enabled in a predetermined system mode, for transmitting an internal signal of the microcontroller to a clock output pin for using the clock output pin and a second switch, which is coupled between the clock generating means and the clock output pin and enabled in the clock generation mode for transmitting the clock signal between the clock generating means and the clock output pin and disabled in the predetermined system mode. As admitted in the Office Action on page 3, Williams fails to disclose, teach, or suggest such a feature. The Office Action alleges that Hui teaches the above features of claim 1. Applicant respectfully disagrees.

Hui merely discloses a test-mode input buffer 44 and a test-mode output buffer 46 between an input pad and an output pad. As shown in Figure 2, Hui discloses that each buffer 44 and 46 is controlled by a TEST_EN signal 41. Specifically, the test-mode input buffer 44 includes a series of gates for receiving the TEST_EN signal to transmit the signal from the input pad to the test-mode output buffer 46 when the TEST_EN signal is activated. The test-mode output buffer 46 is enabled by a NAND gate 72, a NOR gate 75, and two transistors 76 and 77 when the TEST_EN signal is activated. Accordingly, each switch included in each buffer 44 and 46 is enabled in a test mode and disabled in other system

modes. However, in the present invention, a first switch is enabled in a predetermined system mode and a second switch is enabled in the clock generation mode but disabled in the predetermined system mode. Accordingly, no combination of Williams and Hui teach or suggest a microcontroller that includes a first switch, enabled in a predetermined system mode, for transmitting an internal signal of the microcontroller to a clock output pin for using the clock output pin and a second switch, which is coupled between the clock generating means and the clock output pin and enabled in the clock generation mode for transmitting the clock signal between the clock generating means and the clock output pin and disabled in the predetermined system mode, as recited in claim 1.

Claims 2-6 are believed allowable for at least the same reasons presented above with respect to claim 1 by virtue of their dependence upon claim 1. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this rejection.

Allowable Subject Matter

Applicant appreciates the Examiner's indication that claims 7-11 are allowable. In view of the foregoing, Applicant respectfully submits that all of the claims (1-11) are allowable.

Conclusion

Therefore, all objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Should any issues remain unresolved, the Examiner is encouraged to contact the undersigned attorney for Applicants at the telephone number indicated below in order to expeditiously resolve any remaining issues.

Respectfully submitted,

MAYER BROWN ROWE & MAW LLP

By: _____
Yoon S. Ham
Registration No. 45,307
Direct No. (202) 263-3280

YSH/VVK

Intellectual Property Group
1909 K Street, N.W.
Washington, D.C. 20006-1101
(202) 263-3000 Telephone
(202) 263-3300 Facsimile

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